CLAIMS

1. (Currently amended) A method of signal processing, comprising:

converting an optical signal into an electrical signal having an amplitude corresponding to optical power of the optical signal;

sampling the electrical signal using two or more sampling windows contained within a time interval having a one-bit length to generate two or more bit estimate values, wherein sampling the electrical signal comprises:

integrating the electrical signal over a first sampling window to generate a first integration result;

comparing the first integration result with a first decision threshold value to generate a first bit estimate value;

integrating the electrical signal over a second sampling window to generate a second integration result; and

comparing the second integration result with a second decision threshold value to generate a second bit estimate value; and

applying a logical function to the two or more bit estimate values to generate a bit sequence corresponding to the optical signal, wherein applying the logical function comprises applying an "AND" function to the first and second bit estimate values to generate a bit of the bit sequence.

2. (Canceled)

3. (Original) The method of claim 1, wherein:

each sampling window has a width;

the electrical signal has a series of waveforms comprising first and second pluralities of waveforms, wherein each waveform of the first plurality represents a binary "0" and each waveform of the second plurality represents a binary "1"; and

for each sampling window:

a waveform is integrated over the sampling window width to generate a corresponding bit estimate value; and

the sampling window width is selected to reduce contribution of the second plurality of waveforms into integration results corresponding to the first plurality of waveforms.

4. (Canceled)

5. (Currently amended) The method of claim [[4]] 1, wherein the first decision threshold value is different from the second decision threshold value.

6. (Original) The method of claim 1, wherein the optical signal is an optical duobinary signal.

7. (Currently amended) The method of claim 1, comprising:

generating a first clock signal based on the electrical signal;

multiplying a frequency of the first clock signal to generate a second clock signal; and

sampling the electrical signal at a sampling rate corresponding to the second clock signal to generate a bit stream carrying the first and second bit estimate values.

8. (Currently amended) The method of claim 7, comprising:

separating the first and second bit estimate values from the bit stream while discarding all other bits of the bit stream~~; and~~

~~applying an "AND" function to the first and second bit estimate values to generate a bit of the bit sequence~~.

9. (Currently amended) The method of claim 1, comprising:

generating a clock signal based on the electrical signal;

sampling first and second copies of the electrical signal at a sampling rate corresponding to the clock signal, wherein:

the first copy is sampled to generate [[a]] the first bit estimate value;

the second copy is sampled to generate [[a]] the second bit estimate value; and

the first and second copies are sampled with a relative time delay.

10. (Canceled)

11. (Currently amended) An optical receiver, comprising:

a signal converter adapted to convert an optical signal into an electrical signal having an amplitude corresponding to optical power of the optical signal; and

a decoder coupled to the signal converter and adapted to:

(i) sample the electrical signal using two or more sampling windows contained within a time interval having a one-bit length to generate two or more bit estimate values; ~~and~~

(ii) apply a logical function to the two or more bit estimate values to generate a bit sequence corresponding to the optical signal;

(iii) integrate the electrical signal over a first sampling window to generate a first integration result;

(iv) compare the first integration result with a first decision threshold value to generate a first bit estimate value;

(v) integrate the electrical signal over a second sampling window to generate a second integration result; and

(vi) compare the second integration result with a second decision threshold value to generate a second bit estimate value, wherein:

the decoder comprises an "AND" gate adapted to apply an "AND" function to the first and second bit estimate values to generate a bit of the bit sequence.

12. (Canceled)

13. (Original) The receiver of claim 11, wherein the optical signal is an optical duobinary signal.

14. (Currently amended) The receiver of claim 11, comprising:

a decision circuit coupled to the signal converter;

a clock recovery circuit coupled to the signal converter and adapted to generate a first clock signal based on the electrical signal; and

a clock multiplier coupled between the clock recovery circuit and the decision circuit and adapted to multiply a frequency of the first clock signal to generate a second clock signal, wherein

the decision circuit is adapted to sample the electrical signal at a sampling rate corresponding to the second clock signal to generate a bit stream carrying the first and second bit estimate values.

15. (Currently amended) The receiver of claim 14, comprising:

a de-multiplexer having an input port and a plurality of output ports, wherein:

the input port is coupled to the decision circuit;

a first output port is adapted to receive a signal corresponding to the first bit estimate value; and

a second output port is adapted to receive a signal corresponding to the second bit estimate value, wherein the ~~; and~~

~~an~~ "AND" gate is coupled to the first and second output ports ~~and adapted to apply an "AND" function to the first and second bit estimate values to generate a bit of the bit sequence~~.

16. (Currently amended) The receiver of claim 11, comprising:

first and second decision circuits, each coupled to the signal converter; and

a clock recovery circuit coupled between the signal converter and the first and second decision circuits and adapted to generate a clock signal based on the electrical signal, wherein:

each decision circuit is adapted to sample the electrical signal at a sampling rate corresponding to the clock signal;

the first decision circuit is adapted to generate [[a]] the first bit estimate value;

the second decision circuit is adapted to generate [[a]] the second bit estimate value; and

the first and second decision circuits sample the electrical signal with a relative time delay.

17. (Currently amended) The receiver of claim 16, ~~comprising an~~ wherein the "AND" gate is coupled to the first and second decision circuits ~~and adapted to apply an "AND" function to the first and second bit estimate values to generate a bit of the bit sequence~~.

18. (Currently amended) The receiver of claim 16, wherein each decision circuit is adapted to:

integrate the electrical signal over a respective sampling window to generate a[[n]] respective integration result; and

compare the respective integration result with a respective decision threshold value to generate a bit estimate value.

19. (Original) The receiver of claim 18, wherein the first and second decision circuits use different decision threshold values.

20. (Currently amended) An optical communication system, comprising an optical receiver coupled to an optical transmitter via a transmission link, wherein the optical receiver comprises:

a signal converter adapted to convert an optical signal into an electrical signal having an amplitude corresponding to optical power of the optical signal; and

a decoder coupled to the signal converter and adapted to:

(i) sample the electrical signal using two or more sampling windows contained within a time interval having a one-bit length to generate two or more bit estimate values; ~~and~~

(ii) apply a logical function to the two or more bit estimate values to generate a bit sequence corresponding to the optical signal;

(iii) integrate the electrical signal over a first sampling window to generate a first integration result;

(iv) compare the first integration result with a first decision threshold value to generate a first bit estimate value;

(v) integrate the electrical signal over a second sampling window to generate a second integration result; and

(vi) compare the second integration result with a second decision threshold value to generate a second bit estimate value, wherein:

the decoder comprises an "AND" gate adapted to apply an "AND" function to the first and second bit estimate values to generate a bit of the bit sequence.

21. (Canceled)

22. (Original) The system of claim 20, wherein the optical signal is an optical duobinary signal.

23. (Currently amended) The system of claim 20, wherein the optical receiver comprises:

a decision circuit coupled to the signal converter;

a clock recovery circuit coupled to the signal converter and adapted to generate a first clock signal based on the electrical signal;

a clock multiplier coupled between the clock recovery circuit and the decision circuit and adapted to multiply a frequency of the first clock signal to generate a second clock signal, wherein the decision circuit is adapted to sample the electrical signal at a sampling rate corresponding to the second clock signal to generate a bit stream carrying the first and second bit estimate values;

a de-multiplexer having an input port and a plurality of output ports, wherein:

the input port is coupled to the decision circuit;

a first output port is adapted to receive a signal corresponding to the first bit estimate value; and

a second output port is adapted to receive a signal corresponding to the second bit estimate value, wherein the ~~; and~~

~~an~~ "AND" gate is coupled to the first and second output ports~~ and adapted to apply an "AND" function to the first and second bit estimate values to generate a bit of the bit sequence~~.

24. (Currently amended) The system of claim 20, wherein the optical receiver comprises:

first and second decision circuits, each coupled to the signal converter;

a clock recovery circuit coupled between the signal converter and the first and second decision circuits and adapted to generate a clock signal based on the electrical signal, wherein:

each decision circuit is adapted to sample the electrical signal at a sampling rate corresponding to the clock signal;

the first decision circuit is adapted to generate [[a]] the first bit estimate value;

the second decision circuit is adapted to generate [[a]] the second bit estimate value; and

the first and second decision circuits sample the electrical signal with a relative time delay, wherein the ~~; and~~

~~an~~ "AND" gate is coupled to the first and second decision circuits ~~and adapted to apply an "AND" function to the first and second bit estimate values to generate a bit of the bit sequence~~.

25. (New) The system of claim 24, wherein:

each decision circuit is adapted to:

integrate the electrical signal over a respective sampling window to generate a respective integration result; and

compare the respective integration result with a respective decision threshold value to generate a bit estimate value; and

the first and second decision circuits use different decision threshold values.